



TL071C,AC TL072C,AC TL074C,AC

Low Noise, JFET Input Operational Amplifiers

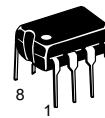
These low noise JFET input operational amplifiers combine two state-of-the-art analog technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input device for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents. Moreover, the devices exhibit low noise and low harmonic distortion, making them ideal for use in high fidelity audio amplifier applications.

These devices are available in single, dual and quad operational amplifiers which are pin-compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar products.

- Low Input Noise Voltage: $18 \text{ nV}/\sqrt{\text{Hz}}$ Typ
- Low Harmonic Distortion: 0.01% Typ
- Low Input Bias and Offset Currents
- High Input Impedance: $10^{12} \Omega$ Typ
- High Slew Rate: $13 \text{ V}/\mu\text{s}$ Typ
- Wide Gain Bandwidth: 4.0 MHz Typ
- Low Supply Current: 1.4 mA per Amp

LOW NOISE, JFET INPUT OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA

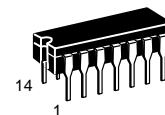
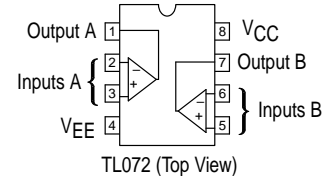
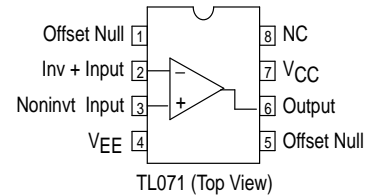


P SUFFIX
PLASTIC PACKAGE
CASE 626



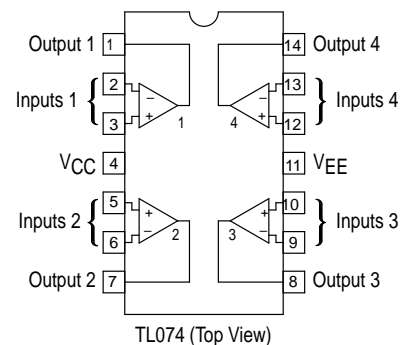
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS



N SUFFIX
PLASTIC PACKAGE
CASE 646
(TL074 Only)

PIN CONNECTIONS



ORDERING INFORMATION

Op Amp Function	Device	Operating Temperature Range	Package
Single	TL071ACD, CD	$T_A = 0^\circ \text{ to } +70^\circ\text{C}$	SO-8
	TL071ACP, CP		Plastic DIP
Dual	TL072ACD, CD	$T_A = 0^\circ \text{ to } +70^\circ\text{C}$	SO-8
	TL072ACP, CP		Plastic DIP
Quad	TL074ACN, CN	$T_A = 0^\circ \text{ to } +70^\circ\text{C}$	Plastic DIP

TL071C,AC TL072C,AC TL074C,AC

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} V_{EE}	+18 -18	V
Differential Input Voltage	V_{ID}	± 30	V
Input Voltage Range (Note 1)	V_{IDR}	± 15	V
Output Short Circuit Duration (Note 2)	t_{SC}	Continuous	
Power Dissipation Plastic Package (N, P) Derate above $T_A = +47^\circ\text{C}$	P_D $1/\theta_{JA}$	680 10	mW mW/ $^\circ\text{C}$
Operating Ambient Temperature Range	T_A	0 to +70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

- NOTES:** 1. The magnitude of the input voltage must not exceed the magnitude of the supply voltage or 15 V, whichever is less.
2. The output may be shorted to ground or either supply. Temperature and/or supply voltages must be limited to ensure that power dissipation ratings are not exceeded.

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = T_{high}$ to T_{low} [Note 3])

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leq 10\text{ k}$, $V_{CM} = 0$) TL071C, TL072C TL074C TL07_AC	V_{IO}	— — —	— — —	13 13 7.5	mV
Input Offset Current ($V_{CM} = 0$) (Note 4) TL07_C TL07_AC	I_{IO}	— —	— —	2.0 2.0	nA
Input Bias Current ($V_{CM} = 0$) (Note 4) TL07_C TL07_AC	I_{IB}	— —	— —	7.0 7.0	nA
Large-Signal Voltage Gain ($V_O = \pm 10\text{ V}$, $R_L \geq 2.0\text{ k}$) TL07_C TL07_AC	A_{VOL}	15 25	— —	— —	V/mV
Output Voltage Swing (Peak-to-Peak) ($R_L \geq 10\text{ k}$) ($R_L \geq 2.0\text{ k}$)	V_O	24 20	— —	— —	V

- NOTES:** 3. $T_{low} = 0^\circ\text{C}$ for TL071C,AC
TL072C,AC
TL074C,AC
 $T_{high} = +70^\circ\text{C}$ for TL071C,AC
TL072C,AC
TL074C,AC

4. Input Bias currents of JFET input op amps approximately double for every 10°C rise in junction temperature as shown in Figure 3. To maintain junction temperature as close to ambient temperature as possible, pulse techniques must be used during testing.

Figure 1. Unity Gain Voltage Follower

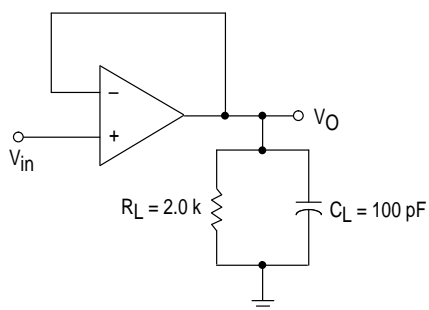
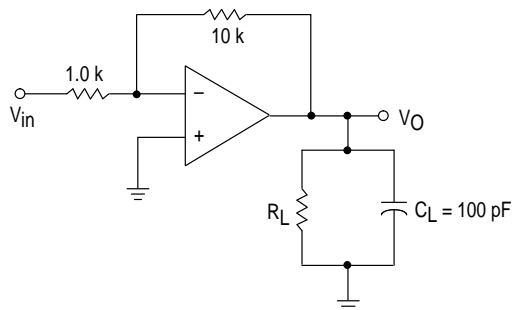


Figure 2. Inverting Gain of 10 Amplifier



TL071C,AC TL072C,AC TL074C,AC

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leq 10\text{ k}$, $V_{CM} = 0$) TL071C, TL072C TL074C TL07_AC	V_{IO}	—	3.0 3.0 3.0	10 10 6.0	mV
Average Temperature Coefficient of Input Offset Voltage $R_S = 50\ \Omega$, $T_A = T_{low}$ to T_{high} (Note 3)	$\Delta V_{IO}/\Delta T$	—	10	—	$\mu\text{V}/^\circ\text{C}$
Input Offset Current ($V_{CM} = 0$) (Note 4) TL07_C TL07_AC	I_{IO}	—	5.0 5.0	50 50	pA
Input Bias Current ($V_{CM} = 0$) (Note 4) TL07_C TL07_AC	I_{IB}	—	30 30	200 200	pA
Input Resistance	r_i	—	10^{12}	—	Ω
Common Mode Input Voltage Range TL07_C TL07_AC	V_{ICR}	± 10 ± 11	+15, -12 +15, -12	— —	V
Large-Signal Voltage Gain ($V_O = \pm 10\text{ V}$, $R_L \geq 2.0\text{ k}$) TL07_C TL07_AC	A_{VOL}	25 50	150 150	— —	V/mV
Output Voltage Swing (Peak-to-Peak) ($R_L = 10\text{ k}$)	V_O	24	28	—	V
Common Mode Rejection Ratio ($R_S \leq 10\text{ k}$) TL07_C TL07_AC	CMRR	70 80	100 100	— —	dB
Supply Voltage Rejection Ratio ($R_S \leq 10\text{ k}$) TL07_C TL07_AC	PSRR	70 80	100 100	— —	dB
Supply Current (Each Amplifier)	I_D	—	1.4	2.5	mA
Unity Gain Bandwidth	BW	—	4.0	—	MHz
Slew Rate (See Figure 1) $V_{in} = 10\text{ V}$, $R_L = 2.0\text{ k}$, $C_L = 100\text{ pF}$	SR	—	13	—	$\text{v}/\mu\text{s}$
Rise Time (See Figure 1)	t_r	—	0.1	—	μs
Overshoot ($V_{in} = 20\text{ mV}$, $R_L = 2.0\text{ k}$, $C_L = 100\text{ pF}$)	OS	—	10	—	%
Equivalent Input Noise Voltage $R_S = 100\ \Omega$, $f = 1000\text{ Hz}$	e_n	—	18	—	$\text{nV}/\sqrt{\text{Hz}}$
Equivalent Input Noise Current $R_S = 100\ \Omega$, $f = 1000\text{ Hz}$	i_n	—	0.01	—	$\text{pA}/\sqrt{\text{Hz}}$
Total Harmonic Distortion V_O (RMS) = 10 V, $R_S \leq 1.0\text{ k}$, $R_L \geq 2.0\text{ k}$, $f = 1000\text{ Hz}$	THD	—	0.01	—	%
Channel Separation $A_V = 100$	CS	—	120	—	dB

NOTES: 3. $T_{low} = 0^\circ\text{C}$ for TL071C,AC TL072C,AC TL074C,AC
 $T_{high} = +70^\circ\text{C}$ for TL071C,AC TL072C,AC TL074C,AC

4. Input Bias currents of JFET input op amps approximately double for every 10°C rise in junction temperature as shown in Figure 3. To maintain junction temperature as close to ambient temperature as possible, pulse techniques must be used during testing.

Figure 3. Input Bias Current versus Temperature

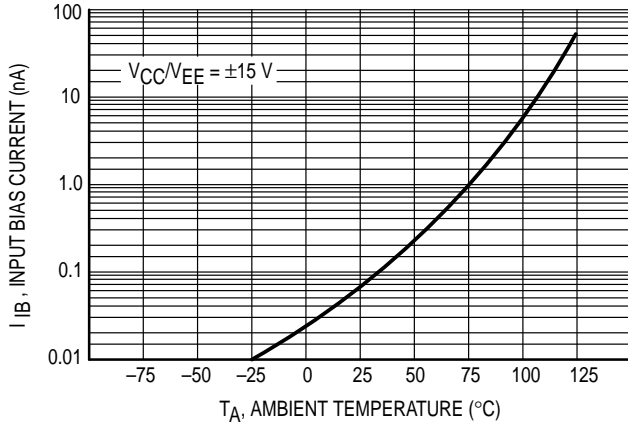


Figure 4. Output Voltage Swing versus Frequency

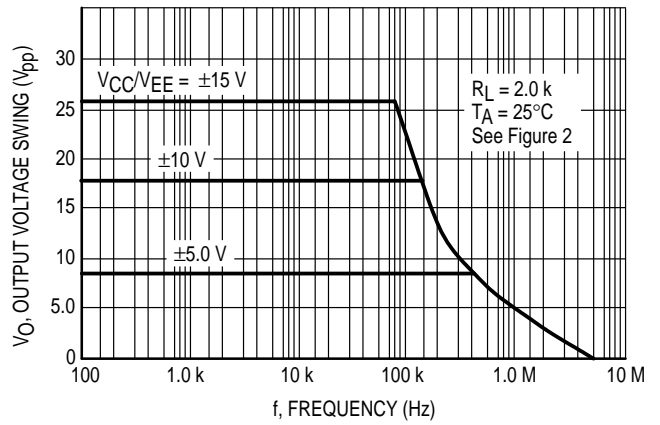


Figure 5. Output Voltage Swing versus Load Resistance

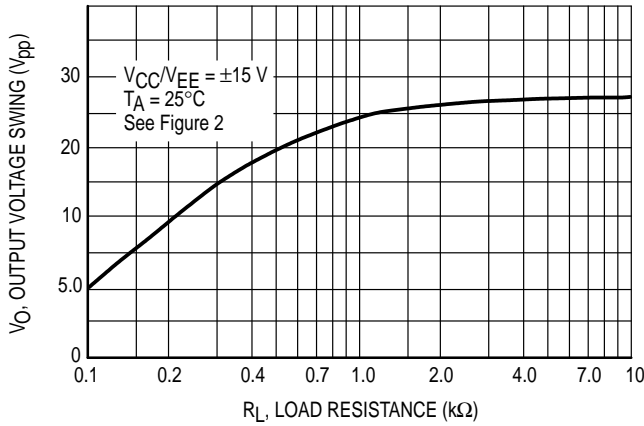


Figure 6. Output Voltage Swing versus Supply Voltage

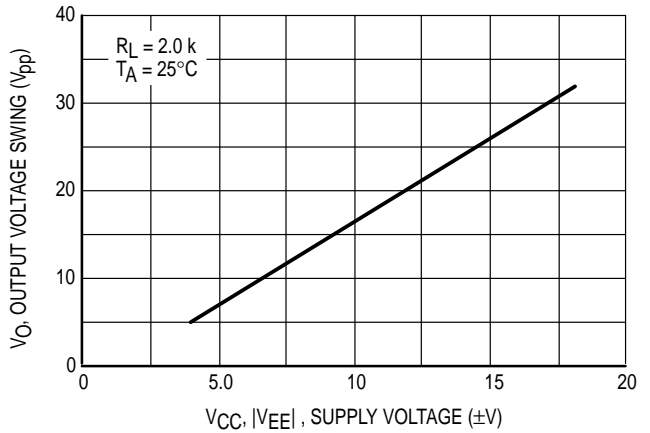


Figure 7. Output Voltage Swing versus Temperature

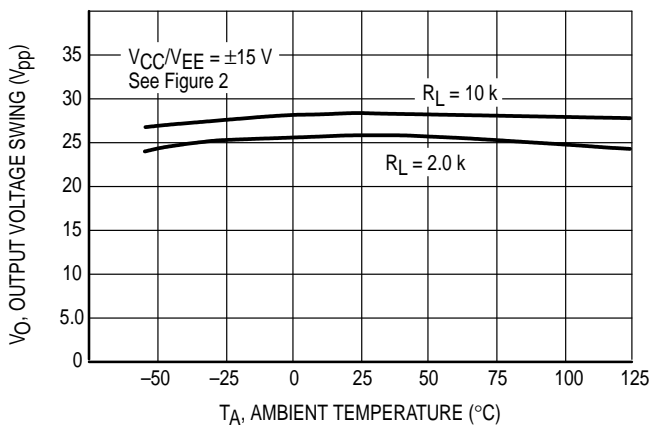


Figure 8. Supply Current per Amplifier versus Temperature

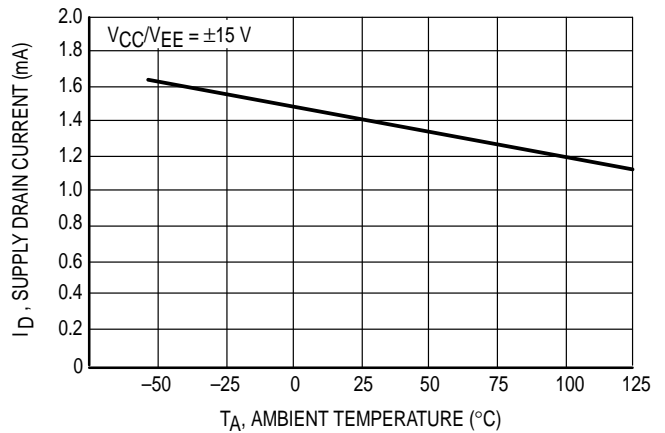


Figure 9. Large Signal Voltage Gain and Phase Shift versus Frequency

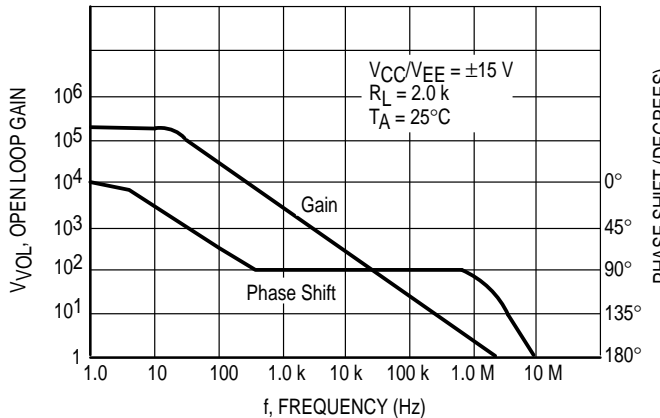


Figure 10. Large Signal Voltage Gain versus Temperature

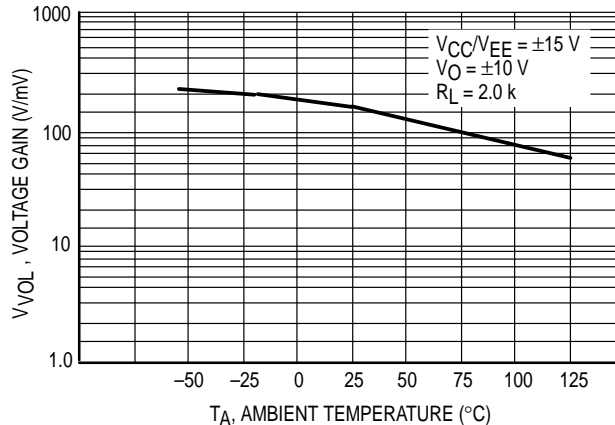


Figure 11. Normalized Slew Rate versus Temperature

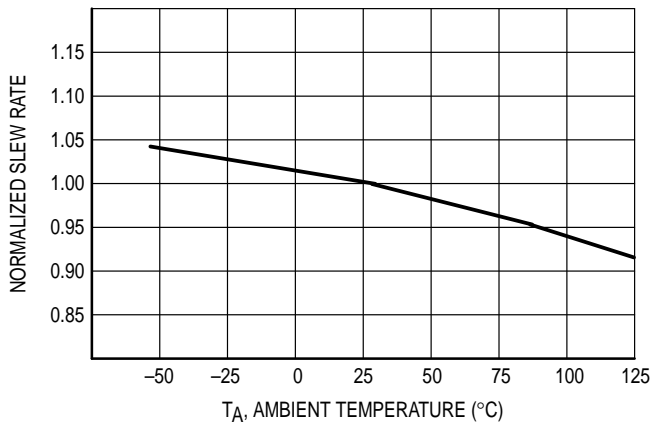


Figure 12. Equivalent Input Noise Voltage versus Frequency

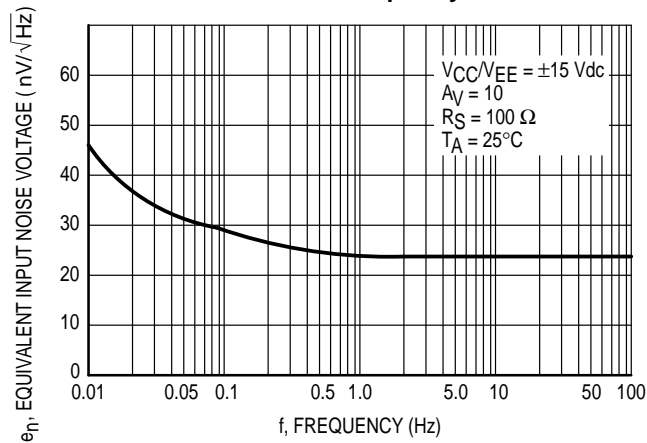
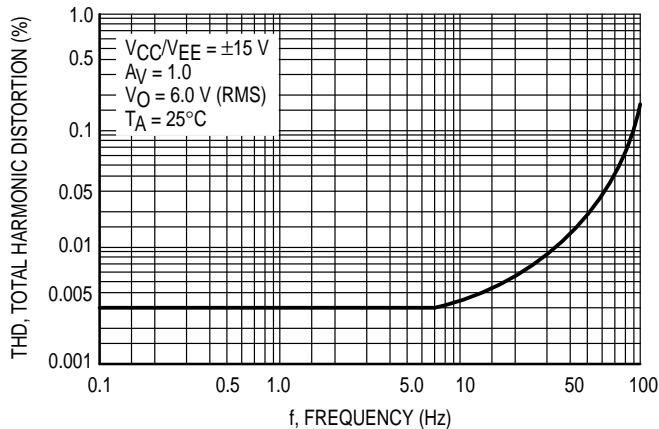


Figure 13. Total Harmonic Distortion versus Frequency



Representative Schematic Diagram
(Each Amplifier)

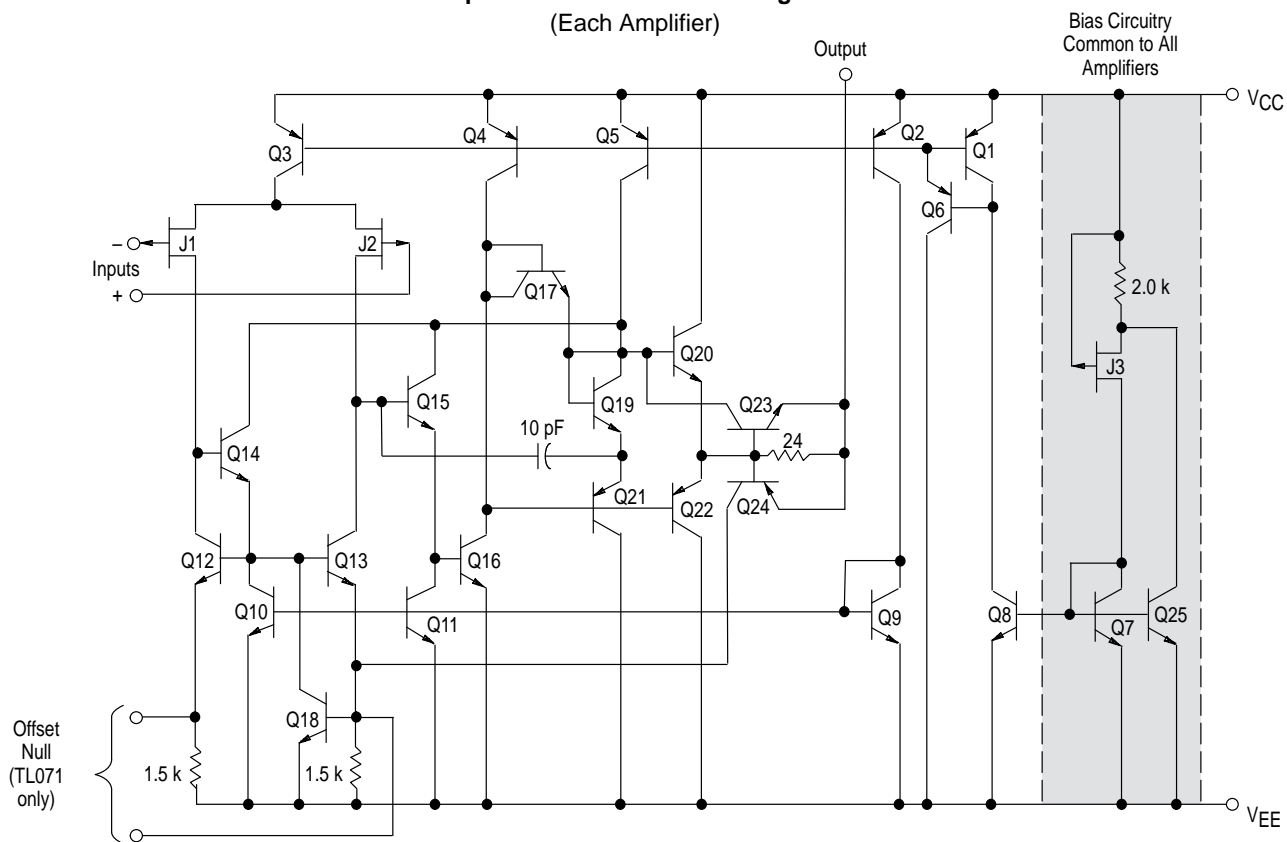


Figure 14. Audio Tone Control Amplifier

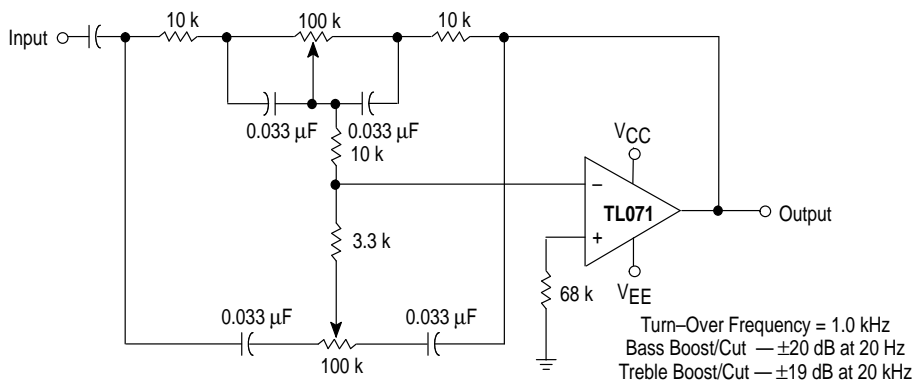
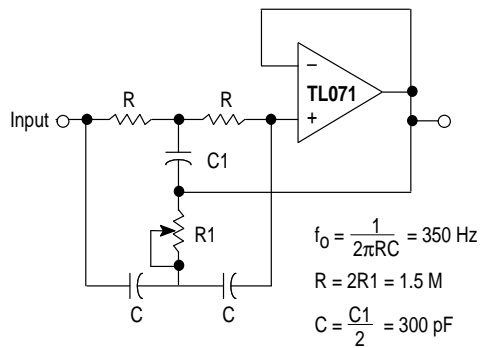


Figure 15. High Q Notch Filter



OUTLINE DIMENSIONS

P SUFFIX
PLASTIC PACKAGE
CASE 626-05
ISSUE K

NOTE 2: [Diagram pointing to lead dimensions]

SEATING PLANE

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	— 10°		— 10°	
N	0.76	1.01	0.030	0.040

⊕ ∅ 0.13 (0.005) (M) T A (M) B (M)

- NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
 3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

D SUFFIX
PLASTIC PACKAGE
CASE 751-05
(SO-8)
ISSUE N

NOTE 2: [Diagram pointing to lead dimensions]

SEATING PLANE

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.009
M	0° 7°		0° 7°	
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

⊕ 0.25 (0.010) (M) T B (S) A (S)

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

N SUFFIX
PLASTIC PACKAGE
CASE 646-06
ISSUE L

NOTE 2: [Diagram pointing to lead dimensions]

SEATING PLANE


	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0° 10°		0° 10°	
N	0.015	0.039	0.39	1.01

⊕ ∅ 0.13 (0.005) (M) T A (M) B (M)

- NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
 2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 4. ROUNDED CORNERS OPTIONAL.

TL071C,AC TL072C,AC TL074C,AC

OUTLINE DIMENSIONS

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TL071/D

